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09/653,156	08/31/2000	Vishnu K. Agarwal	MI22-1518	4650

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EXAMINER

HUYNH, YENNHU B

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 07/11/2003

19

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application N .

09/653,156

Applicant(s)

AGARWAL ET AL.

Examiner

Yennhu B Huynh

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 February 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 and 27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 19.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This Office Action is in response to the Amendment filed on 2/18/03.

Claims 16-26 have been cancelled by Amendment filed on 3/5/02.

#### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title has been as follows: Capacitor Fabrication Method With Increased Surface Area Per Unit Area Of The Substrate.

#### ***Claim Objections***

Claim 2 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 2 recites the limitation which was recited in claim 1 already.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5,8 & 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhodes et al. (U.S. 6,291,289 B2).

Rhodes et al. in related art disclose:

-Re. claims 1,2 & 8: forming a first capacitor electrode comprises TiN monolayer thick 42, 44, 46 (col.2 lines 55-66 , col. 3, and col. 4, lines24-41) over a substrate layer 12, the first electrode having an innermost surface area per unit area and an outermost surface area per unit that are both greater an outer surface area of the surface (fig. 7, col.3, lines 20-23); a capacitor dielectric layer 48 over the first electrode and a second capacitor electrode 50 over the dielectric layer 48.

-Re. claims 3 & 5: forming rugged polysilicon over the substrate and comprises HSG (col.3, lines 12-14) the first electrode 42,44,46 being over the rugged polysilicon (col.3, lines 30-35).

-Re. claim 4: wherein the rugged polysilicon /capacitor first electrode can be is undoped (col.4, lines 37-41)

-Re. claim 9: wherein the dielectric layer comprises Ta2O5 , BST and other dielectric materials can be used (col.3, lines 57-60).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (U.S. 6,174,770B1) in view of Wu (U.S. 6274428B1).

Chi discloses a method for forming a crown capacitor, which include:

-Re. claims 1,3,5,8,10 & 13 forming an opening 113 in an insulating layer 111 over a substrate; the opening having side and bottom (fig.1); forming a polysilicon layer 201 over the side and bottom of opening 113; removing the polysilicon layer over the bottom of the opening (col. 1, 3); converting at least some of the polysilicon layer 201 to HSG (col.3, fig. 2); conformably forming a first capacitor electrode 301 on the converted polysilicon (col.1), the first electrode being sufficiently thin that the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate ((fig,4, col.3); forming a capacitor dielectric 401 on the first electrode and a second capacitor electrode 403 over the dielectric layer.

However, Chi does not disclose a first electrode made of TiN (cls.1,2,14); wherein HSG is undoped (cls. 4,11); converting the polysilicon using a seed (cls. 6,12), the dielectric layer comprises of Ta<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, WO<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub> HfO<sub>2</sub>, BST or ST (cls. 9,15), and wherein the outermost surface area of the first electrode is at least 30% greater than the outer surface area of the substrate (cl. 7).

Wu in related art disclose:

-Re. claims 1,2,14: wherein the first electrode layer 130a made of TiN (col.5, lines 36-38).

-Re. claims 4,11: wherein HSG is undoped (col.5, lines 27-33).

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-Re. claims 6,12: wherein the converting the polysilicon uses a seed (col. 5, lines 33-35)

-Re. claims 9,15: wherein the dielectric layer comprises of Ta<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, WO<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub> HfO<sub>2</sub>, BST or ST (col.7, lines 29-32).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching from Wu 's process in forming a first electrode made of TiN to obtain a large barrier height, and the high constant dielectric layer of Ta<sub>2</sub>O<sub>5</sub>, BST or ST to reduce a leakage current , into Chi's process.

-With respect to claim 7: It is well known in the art to increase a dimension of the surface area of a capacitor. The time, concentration, dimension and thickness are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art, As noted In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to expected that a change in temperature, or in range, concentration, cycles, thickness, would be an unpatentable modification. Under some circumstance, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmischer 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ

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372 (CPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

### ***Response to Arguments***

Applicant's arguments filed on 2/18/03 have been considered but they are not Persuasive.

Applicant argues that:

1) Rhodes et al. do not disclose a first capacitor electrode having an innermost surface area greater than an outer surface area of the substrate.

Chi ('770B1) disclose the first capacitor electrode having an innermost surface area greater than an outer surface area of the substrate, and the conventional HSG silicon formation on a silicon surface is sensitive to the surface doping level and requires precise control of process parameters (figs. 4,5 and col. 3 lines 36-45). In addition, Applicant does not set the parameters of the area of the surface, while Chi also disclose the area directly under capacitor (at fig.5) is the outer surface area because it clearly corresponds with the capacitor. In addition, it is well known to integrate components with large surface areas within smaller areas and Fukuzumi et al. (6,222,722B) also disclose a first capacitor electrode having an innermost surface area greater than an outer surface area of the substrate (figs. 3-8<sup>+</sup>).

2) Rhodes et al. also do not disclose the innermost layer 40 is not constituted a roughened.

Rhodes et al. (col. 3, lines 20,21, fig.5 and col.1, lines 63-66) disclose the layer 42 is also an inner layer to the outer layer 44 and roughened, as well as the capacitor plate comprises an inner and outer surface with a generally roughened surface area.

3) Rhodes et al. also do not disclose that the first capacitor electrode comprising TiN.

Rhodes (col.1, lines 55-63 and the layer 46 is defined as a part of the first capacitor electrode and made of TiN clearly (col.3 & 4 , lines 35-4)

4) Rhodes et al. also do not disclose chemisorbing a layer in forming of the layers 40,42,46 .

Rhodes disclose inherent monolayer forming of 40,42,46 by CVD and through suitable processing outdiffusion of dopant, in manner of one layer thick on another layer. It is well know to make a chemisorption product in forming a monolayer for the first dielectrode (Derderian et al. 6,420,230 B1, col.4, lines9-49).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yennhu Huynh whose telephone number is (703)308-6110. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4.30PM.

If attempts to reach the examiner by telephone are unsuccessfully, the




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examiner's supervisor, Carl Whitehead, can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

YNBH,  
10/4/02

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
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